Title

Hardware accelerated segmentation of CT images for adaptive radiotherapy

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Abstract:

Radiotherapy aims to kill cancer cells by exposing them to radiation. Changes in the position, size and shape of organs between the acquisition of images used to plan the treatment and the treatment delivery can compromise accuracy. Currently, images acquired at the time of treatment are compared to the planning images by clinical staff to ensure that the accuracy of the treatment is within acceptable limits. Adaptive radiotherapy seeks to improve the accuracy of radiotherapy by using images acquired at the time of treatment to adapt the original plan. The image processing and dose calculation steps required to automatically adapt the treatment cannot currently be performed fast enough to make them clinically viable. Hardware acceleration of these algorithms has the potential to make automatic adaptive radiotherapy a clinical possibility.

This paper presents a global thresholding algorithm based on Otsu's method that was used to segment a series of CT images of a test object into three classes. The algorithm was accelerated by implementing sections of it using reconfigurable hardware in the form of a field programmable gate array (FPGA). The execution time of this implementation was compared to implementations running on an ARM Cortex-A9 and an Intel Core-i5 central processing unit (CPU).

The execution times are shown in table 1. The hardware accelerated implementation was found to execute around sixty times as fast as the un-accelerated algorithm. The implementation running on the more powerful Intel CPU was also found to run around 14% slower than the hardware accelerated version.

This work has served as a proof of principle, exhibiting the increases in performance possible by implementing image processing algorithms using dedicated hardware resources. It is intended to extend this work by implementing more complex algorithms and applying these to images used in the treatment of bladder cancer patients.

Images/Diagrams:

Table 1: Algorithm execution times

Implementation	**Execution Time (ms)**
Hardware Accelerated	14.8
ARM Cortex-A9	885.0
Intel Core-i5	17.0

References: